Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Application No.	10/613,628
Filed	7/2/2003
First Inventor	Srinivasan, Varadarajan
Art Unit	2667
Examiner	
Atty. Docket No.	NLMI.P211

Non Patent Literature Documents

Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans-lation
JY	Advanced Traffic Management for Multiservice ATM Networks, www.net.com, Pub. Dec. 15, 2000, (12/15/00), 22 pgs.	
JY	Agere Ads Additional PaloadPlus Processor to Product Line, Agere Press Release, November 29, 2000 (11/29/00), 3 pgs.	
JY	Architecture and Design of Function Specific Wire-Speed Routers for Optical Internetworking, published by Entridia Corp., December 6, 2000 (12/6/00), 60 pgs.	
JY	ATLAS I: A General-Purpose, Single-Chip ATM Switch with Credit-Based Flow Control, IEEE Hot Interconnects IV Symposium Proceedings, Standford, CA, Pub. August 15-17, 1996, 11 pgs.	
JY	CSIX-L1:Common Switch Interface Specification-L1, published by CSIX, August 5, 2000(8/5/2000) , 72 pgs.	

Examiner Signature		Date Considered	1/10/2007

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

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Non Patent Literature Documents		
Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans-lation
JY	Efficient Fair Queuing Using Deficit Round Robin, M Shreedhar, George Varghese, Pub. Date Unknown, 12 pgs.	
JY	genFlow CAN-2500gF OC48c Multiprotocol Traffic Management Coprocessor, Acorn Networks, Pub. Date Unknown, 4 pgs.	
JY	genFlow OC-48c Multiprotocol Traffic Management Coprocessor, Acorn Networks, Pub. Date unknown, 4 pgs.	
JY	Hierarchical Packet Fair Queueing Algorithms, Jon C.R. Bennett, Hui Zhang, Pub. Date Unknown, 14 pgs.	
JY	iFlow Networking using Smart Memory Technology, Silicon Access Networks, Pub. Oct. 2000, 10 pgs.	
JY	Implementation of ATLASI: a Single-Chip ATM Switch with Backpressure, IEEE Hot Interconnects IV Symposium Proceedings, Standford, CA, Pub. August 13-15, 1998, 12 pgs.	
JY	Introduction to ATM Traffic Management, www.net.com, Pub. Dec. 15, 2000 (12/15/00), 15 pgs.	
JY	Network Processing New Concepts Using Smart Memory Technology, Silicon Access Networks, Publ. October 2000, 7 pgs.	
JY	Orologic's Traffi-Shaping Chip Set Handles ATM, IP, TechWeb.com, Nov. 30, 2000 (11/30/00), 2 pgs.	

Examiner Signature		Date Considered	1/10/2007

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Non Patent Literature Documents		
Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans-lation
JY	PaceMaker 2.4 (formerly QoSCore, Orologic Press Release, Nov. 30, 2000 (11/30/00) 1 page	
JY	PaceMaker 2.4 OC-48 Traffic Management Engine, Vitesse Semiconductor Corp., Pub 2000, 2 pgs.	
JY	PayloadPlus Routing Switch Processor, Lucent Technologies, April 2000, 6 pgs.	
JY	PMC-Sierra's ATM Chip Set Provides the Traffic Management and Switch Fabric Core for Ericsson's AXD 301 ATM Switch, PMC-Sierra, Publ. December 12, 2000 (12/12/00), 10 Pgs.	
JY	Scalable Harware Earliest-Deadline-First Scheduler for ATM Switching Networks, 18th IEEE Reeal-Time Systems Symposium, Pub. 1997, 9 pgs.	
JY	Simulation Sutdy of Statistical Delays in an ATM Switch Using EDF Scheduling, Dept. of Computer Science, North Carolina State University, Pub. June 24, 1999 (6/24/99), 25 pgs.	
JY	Smart Memory Technology in the MAN, Silicon Access Networks, Pub. October 2000, 6 pgs	
JY	Smart Memory Technology Target Markets, Silicon Access Networks, Pub. October 2000, 5 pgs.	
JY	Start-time Queuing: A Scheduling Algorithm for Integrated Services Packet Switching Networks, Pawan Goyal, Harrick M. Vin and Haichen Cheng, Distributed Multimedia Computing Laboratory, Dept. Computer Sciences, University of Texas at Austin, Pub. 1996, 12	

Examiner Signature		Date Considered	1/10/07

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

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Non Patent Literature Documents		
Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans-lation
JY	Statistical Delay Bounds Oriented Packet Scheduling Algorithms in High Speed Networks, by Kai Zhu, North Carolina State University, Pub. 2000, 6 pgs.	
JY	Traffic Scheduling in Packet-Switched Networks: Analysis, Design and Implementation, university of California, Santa Cruz, Pub. June 1996 (6/1996), 107 pgs.	
JY	Traffic Stream Processor MXT 4400, Conexant, Pub. Date Unknown, 5 pgs.	
JY	Vitesse Announces Industry's First OC-48c Traffic Management Engine, Vitesse Semiconductor Corp., Sept. 28, 2000 (9/28/00), 2 pgs.	
JY	Vitesse Announces Industry's First OC-48c Traffic Management Engine, Orologic Press Release, Nov. 30, 2000 (11/30/00) 2 pgs.	
JY	WAN Fast Intelligent Router, Silicon Access Netowrks, Pub. Oct. 23, 2000 (10/23/00) 4 pgs.	
JY	WF2Q: Worst-case Fair Weighted Fair Queueing, Jon C.R. Bennett, Hui Zhang, Pub. Date Unknown, 9 pgs.	
JY	What is a Network Processor?, Vitesse Semiconductor Corp., Pub Date Unknown, 4 pgs.	
JY	Wire Speed Quality of Service Over Ethernet, Switchcore, Pub. May 8, 2000 (5/8/00), 19 pgs.	

Examiner Signature		Date Considered	1/10/2007

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Examiner Initials	Name of Author, Title of Item, Date, Page(s), Volume-Issue Number(s), Publisher, City and/or Country where Published	Trans-lation
	ZettaCom Delivers In-Service System Scalability with Highly Integrated OC-192 Hybrid Switch Fabric, biz.yahoo.com, Pub Nov. 11, 2000 (11/29/00), 2 pgs.	
	Zettacom: Hurry Up and Wait, www.lightreading.com, Pub. Nov. 29, 2000 (11/29/00), 2 pgs.	

Examiner Signature		Date Considered	1/18/2007

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.